REMARKS/ARGUMENTS

This case has been carefully reviewed and analyzed in view of the Official Action dated 25 March 2005. Responsive to the objections and rejections made in the Official Action, Claims 1, 2, 3, 4, 5, 9, 10, 11, 12, 13, 14, 17 and 18 have been amended to clarify the language thereof and the combination of elements which form the invention of the subject Patent Application. Additionally, Claims 8 and 19 have been cancelled by this Amendment.

In the Official Action, the Examiner objected to Claims 9 and 17 due to informalities therein. Accordingly, Claims 9 and 17 have been amended to correct those informalities kindly noted by the Examiner. Thus, it is now believed that the Examiner's objection to the claims has been overcome.

In the Official Action, the Examiner rejected Claims 1, 10, 13, 14, 15, 16, 17, and 18 under 35 U.S.C. § 102(b), as being anticipated by Applicant's published Patent Application No. 2002/0079577. The Examiner states that the reference discloses a substrate having a top surface and a bottom surface, a semi-conductor die overlaying the top surface, a first array comprising a first plurality of solder joints and a second plurality of solder joints, mounted on the die surface and projecting downwardly therefrom. The Examiner states that the reference further includes a first plurality of solder joints having a higher melting point than the second plurality of solder joints and a second array comprising a third plurality of solder joints mounted on the top surface connecting the die surface and the top

surface. The Examiner states that the reference discloses a third plurality of solder joints having a higher melting point than the second plurality of solder joints.

It is respectfully submitted that Applicant's prior Patent Application Publication is directed to a semi-conductor package that forms a solder array on each of the die surface and corresponding printed circuit board. The array on the die consists of solder joints 12, 26 and 14, 28 having two sets of melting points and the array on the printed circuit board 16 comprise two sets of solder joints 18, 22 and 20, 24 with different melting points. The solder joints 12, 26 and 18, 22 are formed of a high melting temperature solder, while the solder joints 14, 28 and 20, 24 are formed of low melting temperature solders, page 2, paragraph 38. As clearly shown in Fig. 1, and in fact every other embodiment of the reference, the solder joints formed of high melting temperature solder are disposed in aligned relationship, while the solder joints formed of a low temperature solder are also disposed in respective alignment, such that subsequent to the reflow process, the solder joints 12, 26 and 18, 22, maintain their original shape, as they are unmelted and function as standoffs, while the low temperature solder joints 14, 28 and 20, 24 are integrally joined and form an hourglass-type contour.

Referring now to Appendix Drawing 11, enclosed herewith, there is shown a die 6 having a low temperature solder joint 14 extending therefrom for coupling with the low temperature solder joint 14 of the printed circuit board 8, which is the basic scheme of the reference. Subsequent to the reflow process, as shown in

Figure 11(a), the solder joints 14 melt together and form an hourglass-like structure. Ideally, the hourglass-like contour is uniform and the thinner central diameter sufficiently thick to avoid cracking. However, in actuality, the surface tension of the top pad will drag a portion of the top solder joint upward while the surface tension of the bottom pad combined with gravity will drag most of the low melting solder joint downward. Thus, the low melting solder joints are formed into an hourglass-like structure with a small top portion and an enlarged bottom portion connected by a thin neck intermediate the top and bottom, as shown in Fig. 11(b). This thin neck portion is easily cracked which leads to electrical and mechanical failure.

To solve this problem, the Applicant provides a joint where low temperature solder joints are joined to high temperature solder joints, so that the hourglass-like contour of the low temperature solder extends only from the die surface to the high temperature solder joint, which smaller distance than the prior art arrangement, allows for a thicker neck portion.

Nowhere does Applicant's prior Patent Application Publication disclose or suggest the plurality of first solder joints being respectively contacting a corresponding portion of the plurality of third solder joints and the plurality of second solder joints being melted to be integrally joined to a remaining portion of the plurality of third solder joints, the plurality of second solder joints each having a substantially hourglass contour extending between a corresponding one of the

remaining portion of the plurality of third solder joints and the die surface. Therefore, as the reference fails to disclose each and every one of the elements of the invention of the subject Patent Application, it cannot anticipate that invention. Further, as the reference fails to suggest such a combination of elements, and in fact teaches away from that combination, as it only discloses high temperature solder joints in contact with high temperature solder joints and low temperature solder joints in contact with low temperature solder joints, it cannot make obvious that invention either.

It is believed that each of the dependent claims define further limitations which are patentably distinct, but are at least patentably distinct for the same reasons as the independent claims.

For all the foregoing reasons, it is now believed that the subject Patent Application has been placed in condition for allowance, and such action is respectfully requested.

Respectfully submitted,
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Dated: 26 Sept. 2005

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